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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,195	03/25/2004	Scott D. Willingham	1052-0012	6003

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EXAMINER	
NGUYEN, LONG T	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 01/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/809,195	WILLINGHAM ET AL.
	Examiner	Art Unit
	Long Nguyen	2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☒ Claim(s) *22 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Specification

1. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the first and second transistors are characterized as having an oxide stress voltage less than said first voltage (claims 5 and 14). No new matter should be entered.

Claim Objections

2. Claims 1-7 are objected to because of the following informalities:

Claim 1, line 3, "transistor comprising a" should be deleted for clarity.

Claim 1, line 7, "transistor comprising a" should be deleted for clarity.

Claims 2-7 are objected to because they include the informalities of claim 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-7 and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 1, the recitation "low-voltage transistor" recited on line 3 and 7 is indefinite because "low" is a relative term, so it is unclear at what voltage is considered to be low.

Claims 2-7 and 21 are indefinite because they include the indefiniteness of claim 1.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4, 7-9, 11-13 and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iida (USP 4,906,871).

With respect to claims 1-4, 8, 11-13, 17, 18 and 20, each of Figures 3 and 5-7 of the Iida reference shows a circuit (14), which includes: a capacitor (19) for receiving an input signal (input signal to circuit 14), a first transistor (PMOS Q5), a second transistor (NMOS Q6), an output signal (V2 in Figure 3, the output voltage of circuit 14 in Figures 5-7), and a resistor (R5 in Figure 3, Q7 in Figure 5 in which the resistor is implemented by using NMOS Q7, Q8 in Figure 6 in which the resistor is implemented by using PMOS Q8, and Q7-Q8 in Figure 7 in which the resistor is implemented by using NMOS Q7 and PMOS Q8 connected in parallel), a first power supply voltage (Vcc), a second power supply voltage (Ground), wherein the input signal (input of circuit 14) having a peak-to-peak signal of a first voltage, the difference between the first and second power supply voltages equal to a second voltage (amplitude of signal voltage V2 in Figure 3, amplitude of output signal of circuit 14 in Figures 5-7), and a capacitance of the capacitor (19) is chosen such that the peak-to-peak voltage swing at the control electrodes of the first and second transistors (amplitude of signal voltage V1 in Figure 3, and amplitude of the node at the gates of Q5-Q6 in Figures 5-7) is less than or equal to the second voltage (because of the drop across feedback resistor R5 in Figure 3, Q7 and/or Q8 in Figures 5-7), see Col. 3, lines

30-46 for more detail. The Iida reference does not disclose that the amplitude of level shifter 14 is lower than the amplitude of the input signal of the circuit 14 (i.e., the second voltage is lower than the first voltage). However, it is known in the art that a level shifter is used to interface between two different circuits/systems having different amplitudes. Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify each of the circuit 14 in Figures 3 and 5-7 of the Iida reference by specifically using the input signal of the circuit 14 having an amplitude greater than the amplitude of the output signal of the circuit 14 for the purpose of interfacing between a system having a higher amplitude signal and another system having a lower amplitude signal. Note that the use a level shifter circuit to transform a higher amplitude signal into a lower amplitude signal and vice versa is depending on the needed of the circuit designer for a specific application. This is deemed to be a routine design expedients for those having ordinary skill in the art of CMOS buffer/shifter design. Thus, this modification meets all the limitations of these claims including the second voltage (amplitude of the output voltage) is less than the first voltage (amplitude of the input voltage), and a capacitance of the capacitor (19) is chosen such that the peak-to-peak voltage swing at the control electrodes of the first and second transistors (amplitude of signal voltage V1 in Figure 3, and amplitude of the node at the gates of Q5-Q6 in Figures 5-7) is less than or equal to the second voltage (because of the drop across feedback resistor R5 in Figure 3, Q7 and/or Q8 in Figures 5-7). Note, in the above modification, because the structure of the claims are fully met so it also meets the limitations of method claim 17, i.e., in the modification of circuit 14, the input signal (input of circuit 14) having a first voltage, the second signal (voltage signal at the control terminals of Q5 and Q6) having a second voltage (V1), and because V2 is greater than or

equal to V1 (due to the drop across feedback resistor R5, Q7 and/or Q8) so V1 is less than or equal to the power supply voltage Vcc (because V2 = Vcc – ground 0V in the operation of circuit 14), note that V2 is also less than the voltage at the input of circuit 14 (due to the modification as discussed above).

With respect to claims 9 and 19, each of the modification of circuit 14 in Figures 3 and 5-7 also shows an interconnected line (the output line of circuit 14) having a first end connected to the output terminal of the circuit (i.e., the line coupled to node V2 of circuit 14 in Figure 3, or to the output node in Figures 5-7) and a load (this is inherent because every circuit must have a load coupled thereto, e.g., the load that the circuit is driving or the downstream circuitry) connected to the second end of the interconnected line.

With respect to claims 7 and 16, the modification as discussed in claims 1 and 8 meets all of the limitations of this claim except for the first voltage is 3.5V and the second voltage is 1.2V. However, it is seen that the specific amplitude voltage of an input signal and the specific power supply voltage in a circuitry is a matter design choice for a specific application. Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the above modification so that the input signal having the amplitude of 3.5V (i.e., the first voltage is approximately 3.5V) and the second voltage is approximately 1.2V (i.e., by using the power supply voltage of 1.2V then the second voltage having amplitude of 1.2V) for the purpose of the purpose of interfacing between a system having a 3.5V amplitude signal and another system having a 1.2V amplitude signal and also achieving a specific power consumption of the circuitry. Note that this is deemed to be a routine design expedients for those having ordinary skill in the art of CMOS buffer/shifter design.

7. Claims 5, 6, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iida (USP 4,906,871) in view of Guedon et al. (USP 6,864,736).

With respect to claims 6 and 15, the modification as discussed in claims 1 and 8 above (see section 6) meets all the limitations of these claims except that the first and second transistors having gate oxide thickness that is substantially a minimum thickness of an associated manufacturing process. However, the Guedon et al. reference teaches that a device that use only thin gate oxide transistors providing the advantage of making the device more compact. Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the above modification by using minimum thickness of an associated manufacturing process for the first and second transistors for the purpose of reducing the space/area of the circuitry. Thus this modification meets all the limitations of claims 6 and 15.

Note that, for claims 5 and 14, because of the use of minimum gate oxide thickness, then there is no needed in stressing the gate oxide so the stress voltage of the transistors is the minimum of the associated manufacturing process, so the stress voltage of the first and second transistors is less than the first voltage. This is similar as applicant's invention.

8. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iida (USP 4,906,871) in view of Weste et al. (Principles of CMOS VLSI Design: A Systems Perspective, 2nd edition, pages 207-213).

With respect to claim 10, the modification as discussed in claims 8 and 9 above (see section 6) meets all the limitations of this claim except that the load is a capacitor connected between the second end of the interconnected line and ground. However, the Weste et al. reference teaches that a load capacitor is connected to the output of an integrated circuit for the

purpose of analyzing the rise-time, fall-time and the delay time of the integrated circuit. Therefore, it would have been obvious to one having ordinary skill in the art to modify the above modification (claims 8 and 9) by providing a load capacitor connected to the output of the circuit 14 in Figures 3 and 5-7 of Iida for the purpose of analyzing the rise-time, fall-time and delay time of the circuit.

Allowable Subject Matter

9. Claims 21-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and if rewritten to overcome the indefiniteness set forth above (for claim 21).

Response to Arguments

10. Applicant's arguments filed on 10/25/05 have been fully considered but they are not persuasive.

With respect to the objection to the specification, applicant argues that the specification recites "the voltage swing at node 43 can be reduced to about 1.2V, which is small enough to avoid stressing low voltage transistors 44 and 45". However, this argument is not persuasive because the above recitation is insufficient to construe that the first and second transistors are characterized as having an oxide stress voltage less than said first voltage (claims 5 and 14).

Applicant argues that Iida fails to discloses the first voltage is greater than the second voltage because Iida discloses that the first voltage is 0.4V and the second voltage is 4.4V. However, this argument is not persuasive because the claims are rejected under 103 (not 102), and the 103 rejection clearly discussed the modification of Iida's circuitry so that the first voltage

is greater than the second voltage for the purpose of interfacing between a system having a higher amplitude signal and another system having a lower amplitude signal. Note that the use a level shifter circuit to transform a higher amplitude signal into a lower amplitude signal and vice versa is depending on the needed of the circuit designer for a specific application. This is deemed to be a routine design expedients for those having ordinary skill in the art of CMOS buffer/shifter design.

Applicant also argues that the output voltage V2 of the inverter 14 of Iida is not equivalent to the second voltage as recited in claims 1 and 8 because claims 1 and 8 recite that a voltage difference of the first power supply voltage and the second power supply voltage, i.e., within claims 1 and 8, the second voltage is not indicated to be an output voltage of the buffer but rather the voltage difference between the supply voltages applied to the first and second transistors, so the second voltage does not necessarily appear at the circuit output as suggested by the office action. However, this argument is not persuasive because, in the operation of Iida's circuitry, the second voltage V2 having a voltage swing between the first power supply voltage VCC (when transistor Q5 is ON) and ground 0V (when transistor Q6 is ON) so V2 = VCC – 0V which is the difference between the first and second power supply voltages.

Applicant argues that Iida fails to discloses or suggest a second voltage or a peak-to-peak voltage swing at the control electrodes of the first and second transistors that is less than or equal to the second voltage. However, this argument is not persuasive because the voltage swing at the control of the first and second transistors (Q5-Q6) in the operation of Iida's circuit is less than or equal to the second voltage V2 due the voltage drop across the feedback resistor R5 in Figure 3, Q7 and/or Q8 in Figures 5-7.

Applicant also argues that Iida fails to disclose or suggest either the sizing of capacitor 19 to achieve the reduction in peak-to-peak voltage, or the use of low voltage transistors. However, this argument is not persuasive because the capacitor 19 inherently has a size and the voltage at the control terminals of the first and second transistors is less than or equal to the second voltage which is smaller than the first voltage as discussed in the modification (see section 6), so it meets the limitation of the sizing of the capacitor. With regard to the low voltage transistors, the claims do not recite specifically at what voltage is considered to be low voltage (i.e., how "low" is considered to be low), and the claims also do not recite any other transistors to compare with the low voltage transistors (i.e., there are no other higher voltage transistors in the circuit to differentiate with the low voltage transistors) so for broadest reasonable interpretation, the transistors Q5 and Q6 in Iida's circuitry are considered to be low voltage transistors.

With respect to method claim 17, applicant argues that Iida fails to disclose or suggest a second signal at the second terminal of the capacitor having a peak-to-peak voltage that is less than the first voltage and greater than or equal to the second voltage. However, this argument is not persuasive because the claims are rejected under 103 (not 102), and the 103 rejection clearly discussed the modification of Iida's circuitry so that the first voltage is greater than the second voltage for the purpose of interfacing between a system having a higher amplitude signal and another system having a lower amplitude signal. Note that, in the modification of circuit 14, the input signal (input of circuit 14) having a first voltage, the second signal (voltage signal at the control terminals of Q5 and Q6) having a second voltage (V1), and because V2 is greater than or equal to V1 (due to the drop across feedback resistor R5, Q7 and/or Q8) so V1 is less than or equal to the power supply voltage Vcc (because V2 = Vcc – ground 0V in the operation of circuit

14). Also, note that V2 is also less than the voltage at the input of circuit 14 (due to the modification of circuit 14 as discussed above).

With regard to the arguments regarding Guedon and Iida individually, in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Note that, in the combination of Iida and Guedon, the Guedon reference is used as a secondary reference to support the using of minimum thickness of an associated manufacturing process for the transistors reduces the space/area of the circuitry.

With regard to the arguments regarding Iida and Weste et al. individually, in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Note that, in the combination of Iida and Weste et al., the Weste et al. reference is used as a secondary reference to provide a load capacitor connected to the output of the circuit 14 in Figures 3 and 5-7 of Iida for the purpose of analyzing the rise-time, fall-time and delay time of the circuit.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

12/28/05

LONG NGUYEN
PRIMARY EXAMINER